REMARKS

Claims 33 and 35-37 are amended. Claims 38-40 are added. Claims 33-40 are pending in the application.

Applicant notes that the Disposition of Claims section of the present Office Action incorrectly numbers the pending claims as claims 37-38 and 43-50. Utilizing the correct claim numbering, the list of pending claims should indicate claims 33-37 as pending in the application.

Claims 33-37 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nishimura et al., U.S. Patent No. 5,440,168. The Examiner is reminded by direction to MPEP § 2131 that anticipation requires each and every element of a claim to be disclosed within a single prior art reference. Claims 33-37 are allowable over Nishimura for at least the reason that Nishimura fails to disclose each and every limitation in any of those claims.

As amended independent claim 33 recites forming a fluorine-containing layer proximate a polycrystalline thin film transistor layer, the fluorine-containing layer comprising tungsten. The amendment to claim 33 is supported by the specification at, for example, page 9, lines 10-23. Nishimura discloses implanting fluorine into a polysilicon gate electrode (col 8, lns 24-27), implanting fluorine into a channel polysilicon layer (col 9, lns 48-51), implanting fluorine into the drain region of a polysilicon thin film (col 11, lns 18-21) or implanting fluorine into an active region of a polysilicon thin film (col 11, lns 51-61). The Examiner states at paragraph 1 of page 3 of the present action that Nishimura teaches forming a fluorine-containing layer by CVD using WF_6 and directs attention to Nishimura

at column 7, lines 1-10. Applicant notes that at column 7, lines 1-10, Nishimura discloses CVD formation of a silicon oxide film utilizing N_2 and SiH_4. Nishimura does not disclose or suggest the claim 33 recited forming a fluorine-containing layer proximate a polycrystalline thin film transistor layer, the fluorine-containing layer comprising tungsten. Accordingly, independent claim 33 is not anticipated by Nishimura and is allowable over this reference.

Dependent claims 35 and 36 are amended for clarification purposes. Dependent claims 34-36 are allowable over Nishimura for at least the reason that they depend from allowable base claim 33.

As amended, independent claim 37 recites forming a fluorine-containing layer over a transistor gate and over a polycrystalline thin film transistorlayer. Claim 37 further recites transferring fluorine from the fluorine-containing layer into the polycrystalline thin film transistor layer over the transistor gate. The amendment to independent claim 37 is supported by the specification at, for example, page 13, lines 1-11 and Fig. 8. The Examiner relies on the Nishimura disclosure at Fig. 19 and the accompanying text, and column 11, lines 25-35 to support the anticipation rejection of claim 37. Applicant notes that the implanted fluorine of Fig. 19 is implanted into a layer of resist over the gate layer and as a result is prevented from diffusing into the thin film channel region over the gate (col 11, lns 14-28). Nishimura does not disclose or suggest the claim 37 recited forming a fluorine-containing layer over a transistor gate and over a polycrystalline thin film transistor layer, and transf rring fluorine from the fluorine-containing layer into the polycrystalline thin film transistor layer over the transistor

gate. Accordingly, independent claim 37 is not anticipated by Nishimura and is allowable over this reference.

New claims 38-40 do not add "new matter" to the specification since each is fully supported by the specification as originally filed. Claim 38 is supported by the specification at, for example, page 9, lines 10-23; and page 13, lines 1-11. Claim 39 is supported by the specification at, for example, page 12, lines 12-17. Claim 40 is supported by the specification at, for example, page 9, lines 7-9.

For the reasons discussed above, claims 33-37 are allowable and claims 38-40 are believed allowable. Accordingly, applicant respectfully requests formal allowance of claims 33-40 in the Examiner's next action.

Respectfully submitted,

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Inventor ..... Sandhu et al.
Assignee ..... Micron Technology, Inc.
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Examiner ..... Laura M. Schillinger
Attorney's Docket No. MI22-1780
Title: Method of Forming a Thin Film Transistor

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO APRIL 10, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

33. (Amended) A method of forming a bottom-gated thin film transistor comprising the following steps:

forming a transistor gate;

forming a polycrystalline thin film transistor layer over the transistor gate;

forming a fluorine-containing layer proximate the polycrystalline thin film transistor layer, the fluorine-containing layer comprising tungsten; and

transferring fluorine into the polycrystalline thin film transistor layer from the fluorine-containing layer.

35. (Amended) The method of claim 33 wherein the forming a fluorine-containing layer comprises ~~forming a sacrificial fluorine containing layer over the thin film transistor layer by~~ chemical vapor deposition utilizing WF_6 and SiH_4 precursors.

36. (Amended) The method of claim 35 further comprising, after the transferring fluorine, removing the ~~sacrificial~~ fluorine-containing layer from over the thin film transistor layer.

37. (Amended) A method of forming a bottom-gated thin film transistor comprising the following steps:

forming a transistor gate;

forming a polycrystalline thin film transistor layer over the transistor gate;

forming a fluorine-containing layer over the transistor gate and over the polycrystalline thin film transistor layer;

providing a buffering layer intermediate the thin film transistor layer and the fluorine containing layer; and

transferring fluorine into the polycrystalline thin film transistor layer over the transistor gate from the fluorine-containing layer.

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